FIG. 1

SOURCE CODE — 8

↓

COMPILER/ASSEMBLER — 9

↓

EXECUTABLE CODE — 10

LC — LC — LC — 16

HOST SYSTEM

12-F

EMULATOR$_2$ — 12-2

EMULATOR$_F$

TC_2

TC_F

13-1

14-1

13-2

14-2

13-F

| OPERATING SYSTEM$_1$ | OPERATING SYSTEM$_2$ | 14-F | OPERATING SYSTEM$_F$ |
| HARDWARE SYSTEM$_1$ | HARDWARE SYSTEM$_2$ | 15-F | HARDWARE SYSTEM$_F$ |

15-1

• • •

15-2

FIG. 2

L C — 16

HOST SYSTEM — 24

| GROUP ACCESS | LC$_G$ → | LEGACY CODE TRANSLATOR | → | TRANSLATOR STORE |

10 — 21

↓

TABLE

23

↓

TRANSLATED CODE CACHE

22

13-F

EXECUTION UNIT ← TC_F

Atty: David E. Lovejoy
Tel No: 415-362-3800

Atty Doc No: AMDH-08152US0 DEL
Inventor 1: Ronald Hilton
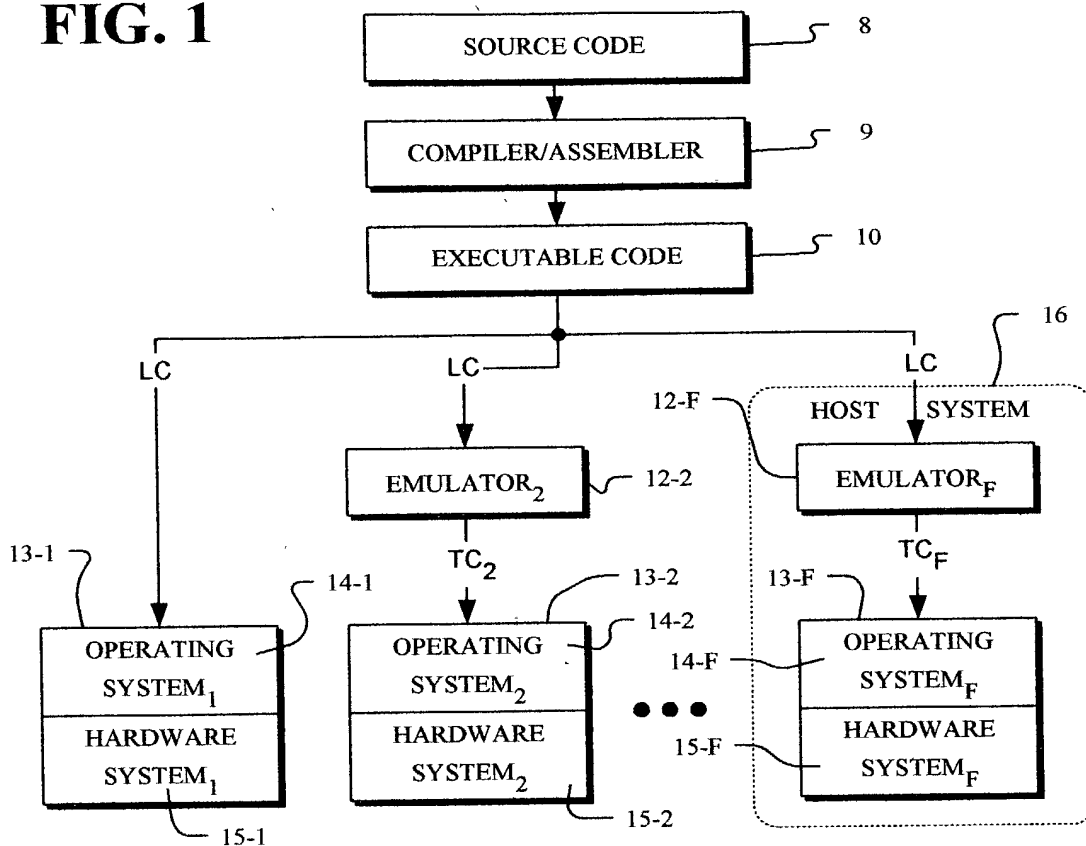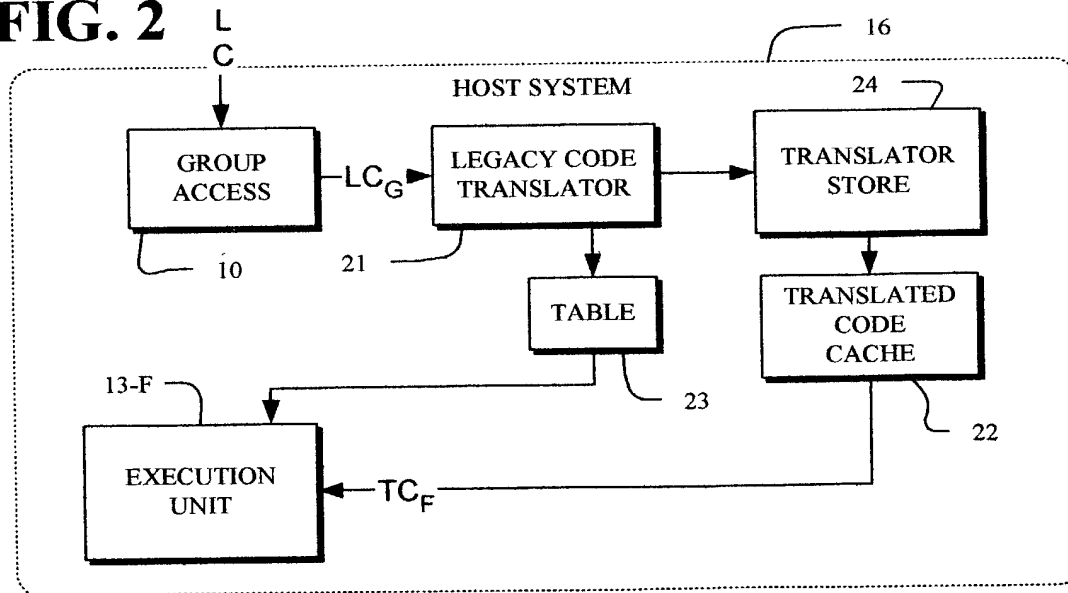Title: PROCESSING OF SELF-MODIFYING CODE UNDER EMULATION

SC/Serial No. 09/992,130
Date Filed: 11/14/2001

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LEGACY CODE (CISC)

```
100   START   BALR   B1,R0
102   BASE    LM     R1,R2,DATA1
106           MVC    DATA1, DATA3
10C           AH     R1,DATA2
110           SRA    R1,1
114           SH     R2,DATA2
118           AR     R1,R2
11A           BC     TARGET
120   DATA1   DC     X'005390BC'
              DC     X'09C20004'
128   DATA2   DC     X'0009'
12A   DATA3   DC     X'800039AF'
```

FIG. 3

```
100   START   BALR   B1, R0
102   BASE    LM     R1, R2,DATA1
106           MVC    DATA1, DATA3
10C           AH     R1, DATA2
```

TRANSLATED CODE (RISC)

```
BALR MOV  B1  BASE
LM   ADD  A1  B1,DATA1 - BASE
     LD4  R1  [A1]
     ADD  A1  A1,4
     LD4  R2  [A1]
MVC  ADD  A1  B1,DATA1-BASE
     ADD  A2  B1,DATA3-BASE
     LD4  T1  [A2]
     ST4  T1  [A1]
AH   ADD  A1  B1,DATA2 -BASE
     LD2  T1  [A1]
     ADD  R1  R1,T1
     B        XFER_SEQUENTIAL
```

```
110           SRA    R1,1
114           SH     R2,DATA2
118           AR     R1,R2
11A           BC     TARGET
120   DATA1   DC     X'005390BC'
              DC     X'09C20004'
128   DATA2   DC     X'0009'
12A   DATA3   DC     X'800039AF'
```

```
SRA  SHR  R1  1
SH   ADD  A1  B1,DATA2 -BASE
     LD2  T1  [A1]
     SUB  R2  R2,T1
AR   ADD  R1  R1,R2
BC   ADD  A1  B1,TARGET - BASE
     B        XFER_BRANCH
```

Atty David E. Lovejoy
Tel No: 415-362-3800

Atty Doc No: AMDH-08152US0 DEL   SC/Serial No: 09/992,130

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FIG. 4